REMARKS

Claims 1, 3-5, 14, 16-18, 27 and 29 are amended. Claims 2, 15, and 28 are cancelled. The elements of claims 2, 15, and 28 are incorporated into claims 1, 14 and 27, respectively. Claims 1, 3-14, 16-27 and 29-39 are pending in the present application.

Claims 1, 14 and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,776,645 ("Barr"). Applicants respectfully traverse this rejection.

Claim 1, as amended, recites a method for measuring the registration between at least two integrated circuit layers comprising, *inter alia*, "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location" and "determining if said relative location is within stored acceptable design limits for said integrated circuit layers by comparing said relative location to said stored acceptable design limits." Barr does not disclose all of these limitations.

Barr discloses using an "isolated edge detection windows, e.g., detection window 132, . . . where the overlay measurement system searches for an isolated edge" and "adding the measurement for the isolated edge in detection window 132 to the measurement for the isolated edge in detection window 127 and dividing the sum by 2." Col. 4, lines 5-16; Fig. 20. Barr discloses that the "average center of print bias target 16 is found by first finding the midpoint between the isolated edges within detection windows 123 and 125," and that this is "merely an average of the measurements for those isolated edges." Col. 14, lines 16-19; Fig. 20. Thus, Barr discloses calculating an average measurement or "average center" between two features, and not "determining a location of a first feature reference point in said visible feature of one of said layers."

Likewise, claim 14, as amended, recites, *inter alia*, a "means for digitizing said image and processing said digitized image to *determine a location of a first feature reference point in said visible feature of one of said layers*, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers." (Emphasis added).

Claim 27, as amended, recites, *inter alia*, "digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer by *determining a location of a first feature reference point in said first visible feature of said first integrated circuit layer*, and a location of a second feature reference point in said second visible feature of said second integrated circuit layer to indicate said relative location." (Emphasis added). Barr does not disclose either limitation of claim 14 or of claim 27.

Since Barr does not disclose all the limitations of claims 1, 14 and 27, Barr does not anticipate these claims. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(b) rejection of claims 1, 14, and 27 be withdrawn.

Claims 1, 3-9, 11-14, 16-22, 24-27, 29-35 and 37-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "the combination of Into (US 4,938,600A) and Barr et al. (US 5,776,645A)." Applicants respectfully traverse this rejection.

Into and Barr, whether considered alone or in combination, do not teach or suggest all the limitations of claim 1. In particular, Into and Barr, even when considered together, fail to teach or suggest "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second

feature reference point in said visible feature of the other of said layers, to indicate a relative location" or "determining if said relative location is within stored acceptable design limits for said integrated circuit layers by comparing said relative location to said stored acceptable design limits," as recited in claim 1.

Into discloses a method "for measuring displacement between layers of a semiconductor wafer wherein systematic errors associated with the measurement system are eliminated." (Abstract). The Into method comprises "making a first measurement of displacement between the first pattern and the second pattern, causing rotation of the workpiece and the measurement apparatus relative to each other by substantially 180° about an axis that is substantially parallel to the measurement direction, making a second measurement of displacement between the first pattern and the second pattern, and determining an actual displacement between the first pattern and the second pattern from the first measurement and the second measurement." Col. 2, lines 37-47. Into does not teach or suggest the actual *method of measuring displacement.* At best, Into only discloses that the "measurement of displacement between patterns utilizes known signal processing techniques," such as "by an analysis of signals from camera 22." Col. 4, lines 52-55. Into discloses that the "lines of patterns 50 and 54 each produce a transition in a scan line signal from camera 22," and that the "time interval between a transition corresponding to pattern 54 and a transition corresponding to pattern 50 is representative of the distance between the patterns." Col. 4, lines 52-60; Fig. 3A. Hence, the Into method only teaches a new method to eliminate systematic errors in a measurement system, and not a "method for measuring the registration between at least two integrated circuit layers, one residing over the other," much less a method having all the limitations of claim 1.

Like Barr, Into also does not teach a "system for measuring the registration between at least two integrated circuit layers, one residing over the other" as recited in claim 14. Moreover, Into neither Into nor Barr teach or suggest a "means for digitizing said image and processing said digitized image to determine a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers," as recited in claim 14.

Similarly, even when considered in combination, Into and Barr fail to teach or suggest a "method for measuring the registration between integrated circuit layers," having all the limitations of claim 27. Specifically, Barr does not teach or suggest "digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer by determining a location of a first feature reference point in said first visible feature of said first integrated circuit layer, and a location of a second feature reference point in said second visible feature of said second integrated circuit layer to indicate said relative location," as recited in claim 27.

Since Into and Barr do not teach or suggest all the limitations of claims 1, 14 and 27, these claims and claims 3-9, 11-13, 16-22, 24-26, 29-35 and 37-39 depending therefrom are patentable over the references. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1, 3-9, 11-14, 16-22, 24-27, 29-35 and 37-39 be withdrawn.

Claims 10, 23, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Into and Barr, and further in combination with U.S. Patent No. 4,766,311 ("Seiler"). Applicants respectfully traverse this rejection.

Claim 10 depends from claim 1. Claim 23 depends from claim 14. Claim 36 depends from claim 27. As discussed above, Into and Barr do not teach or suggest all the limitations of claims 1, 14 and 27. Seiler does not supplement the deficiencies of Into and Barr in this respect. Seiler discloses a method and apparatus for "making precise measurements as small as in submicron distances of an object." (Abstract).

Like Into and Barr, Seiler does not teach or suggest all limitations of any of claim s 1, 14, and 27. Specifically, Seiler fails to teach or suggest "determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location" or "determining if said relative location is within stored acceptable design limits for said integrated circuit layers by comparing said relative location to said stored acceptable design limits," as recited in claim 1. Seiler also fails to teach or suggest a "means for digitizing said image and processing said digitized image to determine a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers," as recited in claim 14. Seiler further fails to teach or suggest "digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer by determining a location of a first feature reference point in said first visible feature of said first integrated circuit layer, and a location of a

second feature reference point in said second visible feature of said second integrated circuit layer to indicate said relative location," as recited in claim 27.

Since Into, Barr and Seiler do not teach or suggest all the limitations of claims 1, 14 and 27, these claims and claims 10, 23 and 36 depending therefrom are patentable over the references. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 10, 23 and 36 be withdrawn.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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